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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,372	01/27/2004	Richard Westhoff	ASC-066	1594

51414 7590 03/21/2007

GOODWIN PROCTER LLP
PATENT ADMINISTRATOR
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EXAMINER	
MALSAWMA, LALRINFAMKIM HMAR	
ART UNIT	**PAPER NUMBER**
2823	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/765,372	WESTHOFF ET AL.	
	Examiner	Art Unit	
	Lex Malsawma	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52 and 76-81* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *35, 45-52,80 and 81* is/are allowed.

6)☒ Claim(s) *1-34,36-44 and 76-79* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-34, 36-44 and 76-79 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In the amendment filed 19 December 2006, applicants amended independent claims 1, 2, 16, 26 and 31 to each include the limitation of: annealing the semiconductor layer to reduce the initial compositional variation throughout the semiconductor layer by diffusing at least one of the at least two elements throughout the semiconductor layer. The examiner finds NO support for this limitation in the specification as originally filed; accordingly, the limitation added by amendment constitutes new matter, which must be removed from the claims. Claims 1-34, 36-44 and 76-79 are currently examined with the new matter removed, i.e., Claims 1-34, 36-44 and 76-79 are currently rejected under the same grounds presented in the prior Office action, mailed 19 September 2006.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1, 4-9, 23-25, 37, 38 and 76-79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schaake et al. (4,960,728; hereinafter "**Schaake**") in view of Nakamura et al. (US 2004/0060518 A1; hereinafter "**Nakamura**") and Kao et al. (5,415,128; hereinafter "**Kao**").

Regarding claims 1 and 4-9:

Schaake discloses a method for forming a semiconductor structure, the method comprising:

providing a substrate (not shown, e.g., note Col. 2, lines 26-28);

forming a semiconductor layer 12 (Fig. 1) over a top surface of the substrate, the semiconductor layer including at least two elements (Te, Hg, Cd) that are distributed to define an initial compositional variation within the semiconductor layer (Col. 2, lines 21-45);

annealing the semiconductor layer to reduce the initial compositional variation (Fig. 2 and Col. 3, lines 33-39);

the initial compositional variation varies periodically within the semiconductor layer in a direction perpendicular to a semiconductor layer deposition direction (i.e., note elements 14 and 16 in Fig. 1);

the initial compositional variation defines a column within the semiconductor layer 12, the column having a width and a period (note the width and period of either "14" or "16");

the columnar period being less than approximately 2000 or 1000 nanometers (i.e., less than 20,000 or 10,000 angstroms, note Col. 2, lines 31-33, wherein element "14" has a thickness of about 1000-3000 angstroms and element "16" is a few hundred angstroms thick); and

the semiconductor layer is annealed at an annealing temperature and for a duration sufficient to diffuse at least one of the two elements (Cd or Hg, note Fig. 2) through a diffusion length at least equal to a quarter of the columnar period, i.e., Schaake discloses the annealing step homogenizes the semiconductor film 12, accordingly, the at least one element (Cd or/and Hg) would diffuse throughout the columnar period.

Schaake **lacks** rotating the substrate during the formation of the semiconductor layer, wherein the initial compositional variation is caused by the rotation. However, it is important to note Schaake specifies that the semiconductor layer is formed by MBE or MOCVD (note Col. 1, lines 63-65).

Nakamura **teaches** (in sections 0005, 0006 and 0009) it was well known in the art to rotate a substrate during deposition by MOCVD in order to obtain a more uniform growth. Nakamura further teaches that some non-uniformity in the semiconductor layer occurs even with the implementation of rotation (e.g., note the last sentences in each of sections 0007 and 0010).

Kao **teaches** it was well known in the art that MBE (Molecular Beam Epitaxy) incorporates substrate rotation (e.g., see Col. 1, lines 21-40), and Kao essentially discloses the optimal rotation speed (60 rpm or more), necessary to obtain compositional uniformity, is typically not possible due to practical considerations such as sample mounting, impurity control, etc. (see Col. 1, lines 35-40). In other words, Kao essentially teaches/shows that MBE typically incorporates substrate rotation, however, the typical rotation speed is considerably less than an optimum rotational speed needed to obtain compositional uniformity; accordingly, MBE generally produces a layer with compositional variation even though the substrate is rotated, and the compositional variation would be at least partially due to the rotation speed of the substrate.

In sum, it would have been obvious to one of ordinary skill in the art to modify Schaake by specifically rotating the substrate because both Nakamura and Kao teach/show that incorporating substrate rotation, when performing the deposition processes (MBE or MOCVD) disclosed by Schaake, produces a "more uniform" composition, wherein an initial compositional variation obtained by the deposition processes is at least partially caused by the rotation of the substrate during deposition processes.

Regarding claims 23 and 25:

Schaake discloses the top surface of the semiconductor layer 12 is planarized while the semiconductor layer is annealed (Col. 3, lines 43-45).

Regarding claim 24:

Schaake discloses (in Fig. 2) forming a layer 22 on the top surface of the semiconductor layer 12 prior to annealing, wherein the layer 22 provides a planarized top surface; accordingly,

Schaake discloses the top surface of the semiconductor layer is planarized before the semiconductor layer is annealed.

Regarding claims 37 and 38:

Schaake discloses (in Fig. 1) the semiconductor layer 12 has an undulating surface 20 that is formed during deposition (Col. 2, lines 13-32).

Regarding claims 76-79:

Nakamura discloses (in section 0009) the source gases are injected into the reaction chamber from one of the sidewalls of the chamber; accordingly, the reactor is a horizontal flow deposition chamber and the reactor would be a single wafer reactor. Nakamura further discloses (in section 0010) when utilizing such a "horizontal flow" deposition chamber, the rotation of the substrate essentially results in highest concentration of reactants disposed on the leading edges of the substrate; accordingly, Schaake modified by utilizing a horizontal flow deposition chamber would result in higher fraction of a first element of the semiconductor layer disposed in a leading edge of the substrate. With respect to claim 79, the column would essentially comprise a graded composition wherein the highest concentration would be disposed on the leading edges, as taught by Nakamura; therefore, the "graded" column could be readily described as "a graded column" comprising a high concentration of a first element (located at the leading edge of the substrate), the compositional variation (within the "graded" column) defines a second column within the semiconductor layer, and the second column comprises a low concentration of the first element. In other words, claim 79 is considered to contain limitations for a graded column that is formed when Schaake's method is performed using a horizontal flow deposition chamber (as taught by Nakamura).

6. Claims 1-3, 21, 22 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bedell et al. (6,841,457 B2; hereinafter "**Bedell**") in view of **Kao** (5,415,128).

Regarding claims 1, 2, 21 and 22:

Bedell discloses a method for forming a semiconductor structure, the method comprising: providing a substrate ("14/12/10" in Fig. 1A);

forming a semiconductor layer 16 over a top surface of the substrate (Fig. 1B), the semiconductor layer including at least two elements (silicon and germanium), the elements being distributed to define an initial compositional variation within the semiconductor layer (Col. 6, lines 35-46); and

annealing the semiconductor layer to reduce the initial compositional variation (Col. 8, lines 13-23 and Figs.1B-1D). NOTE: Bedell discloses the annealing permits relaxation of the strained SiGe alloy and that the relaxation anneal may be performed separately form the interdiffusion anneal or combined in one annealing process, i.e., the relaxation anneal at very least reduces the initial compositional variation of the strained SiGe alloy. *Specifically regarding claim 2:* Bedell discloses the substrate has a first lattice constant (i.e., the substrate comprises layer "14', which is single crystal silicon, e.g., note Col. 6, line 37), the semiconductor layer 16 has a second lattice constant (i.e., layer "16" is a SiGe alloy layer, e.g., note Col. 6, lines 35-39), and the first lattice constant differs from the second lattice constant, i.e., the lattice constant of single crystal silicon differs from the lattice constant of a silicon-germanium layer.

Kao **teaches** it was well known in the art to rotate a substrate during a deposition process for forming a semiconductor layer comprised of materials (Si, Ge) similar to those deposited by Bedell (note Kao, Col. 2, lines 20-24). Kao further teaches that one of the deposition processes

specifically mentioned by Bedell (e.g., MBE, see Bedell, Col. 6, line 61) is well known in the art for incorporating substrate rotation (e.g., see Kao, Col. 1, lines 21-40), wherein the rotation provides a more uniform composition of the deposited materials.

It would have been obvious to one of ordinary skill in the art to modify Bedell by rotating the substrate when specifically utilizing MBE because Kao teaches rotating a substrate during deposition by MBE provides a more uniform growth.

Regarding claim 3:

Bedell discloses a first element (silicon) has a first concentration, x, a second element (germanium) has a second concentration, 1-x, and each of the first and second concentrations is at least 5%. Note in column 6 (lines 45-46), Bedell discloses the germanium concentration is preferably from about 10 to 35 percent, accordingly, the silicon concentration would be about 90 to 65 percent.

Regarding claim 42:

Bedell discloses forming a protective layer 18 over the semiconductor layer 16 prior to annealing the semiconductor layer (Col. 7, lines 1-4).

7. Claims 1 and 10-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamane et al. (4,914,488; hereinafter "**Yamane**") in view of **Kao** (5,415,128).

Regarding claims 1 and 10-15:

Yamane discloses a method for forming a semiconductor structure, the method comprising:

providing a substrate 1 (Fig. 5A and Col. 8, line 45);

forming a semiconductor layer 5/6 over a top surface of the substrate (Fig. 5B), the semiconductor layer including at least two elements (Al, Ga, As, or Si), the elements being distributed to define an initial compositional variation within the semiconductor layer (Col. 8, lines 50-54, 60-68; and Col. 9, lines 1-28);

the initial compositional variation varies in a direction parallel to a semiconductor layer deposition direction and defines a superlattice having a periodicity, wherein the periodicity is less than approximately 10 nanometers (e.g., 2.5 nm, note Col. 9, lines 23-25); and

annealing the semiconductor layer to reduce the initial compositional variation, wherein the annealing is performed at a temperature and for a duration sufficient to diffuse at least one of the two elements through a diffusion length at least equal to a quarter-period of the superlattice (i.e., the annealing causes mutual diffusion to transform the superlattice into a continuous layer, see Col. 5, lines 57-61 and Col. 7, lines 15-28).

Yamane **lacks** rotating the substrate during the formation of the semiconductor layer. However, it is important to noteYamane specifies that the semiconductor layer is formed by MBE (e.g., see Col. 5, lines 32-34 or Col. 7, lines 46-47).

Kao **teaches** it was well known in the art that MBE (Molecular Beam Epitaxy) incorporates substrate rotation (e.g., see Col. 1, lines 21-40), wherein the rotation provides a more uniform composition of the deposited materials.

It would have been obvious to one of ordinary skill in the art to modify Christiansen by rotating the substrate because Kao teaches rotating a substrate during deposition by MBE provides a more uniform growth.

8. Claims 16-20 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Christiansen et al. (6,515,335 B1; hereinafter "**Christiansen**") in view of **Kao** (5,415,128).

Regarding claims 16-20:

Christiansen discloses a method for forming a semiconductor structure, the method comprising:

providing a substrate ("10/20/30/40" in Fig. 1A);

forming a semiconductor layer 50/60 over a top surface of the substrate (Fig. 1A), the semiconductor layer including at least two elements (silicon and germanium), the elements being distributed to define an initial compositional variation within the semiconductor layer (Col. 5, lines 18-30 and Col. 6, lines 5-15);

annealing the semiconductor layer to reduce the initial compositional variation, thereby obtaining a homogeneous, uniform composition layer 70 (Col. 6, lines 42-46; the paragraph bridging Cols. 6-7; and Col. 2, lines 53-60);

the annealing temperature (800-1250 °C, note Col. 6, lines 50-52) being greater than the deposition temperature (e.g., 550-700 °C, note Col. 5, lines 28-29), wherein the semiconductor layer may be annealed at a temperature as low as 400 °C (Col. 6, lines 47-50), which is below a melting point of the semiconductor layer and is less than about 1270 °C.

Christiansen **lacks** rotating the substrate during the formation of the semiconductor layer. However, it is important to note Christiansen specifies that the semiconductor layer is formed by MBE (or CVD, see Col. 5, lines 18-21).

Kao **teaches** it was well known in the art that MBE (Molecular Beam Epitaxy) incorporates substrate rotation (e.g., see Col. 1, lines 21-40), wherein the rotation provides a more uniform composition of the deposited materials.

It would have been obvious to one of ordinary skill in the art to modify Christiansen by rotating the substrate because Kao teaches rotating a substrate during deposition by MBE provides a more uniform growth.

Regarding claim 41:

Christiansen discloses an optional graded layer 65 may be incorporated (Col. 8, lines 1-7), wherein the graded layer 65 is formed below the semiconductor layer 70 (Fig. 3) and is acquired by the annealing process, which formed the relaxed, homogenous/uniform composition layer 70; accordingly, layer "65' is a relaxed graded layer formed over the substrate.

9. Claims 1, 23 and 26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malik et al. (US 2004/006744 A1; hereinafter "**Malik**") in view of **Kao** (5,415,128).

Regarding claims 1, 23, 26 and 27:

Malik discloses (in Fig. 1 and paragraphs 0013-0016) a method for forming a semiconductor structure, the method comprising:

providing a substrate;

forming a semiconductor layer over a top surface of the substrate, the semiconductor layer including at least two elements (silicon and germanium), the elements being distributed to define an initial compositional variation within the semiconductor layer (i.e., the initial compositional variation provides a strained film);

annealing the semiconductor layer to reduce the initial compositional variation, thereby providing a relaxed SiGe film;

planarizing a top surface of the SiGe film by chemical-mechanical polishing (CMP).

Although Malik does not specifically recite that the annealing step reduces the initial compositional variation, the annealing process performed to relax the SiGe film will reduce the initial compositional variation in at least some portions of the SiGe film in order to obtain the relaxed SiGe film, i.e., the elements (Ge, Si) redistribute through out the layer to obtain the relaxed film (e.g., note Figs. 3A-3B) wherein the redistribution at very least results in reducing the initial compositional variation in some portions of the semiconductor layer, otherwise, the structure shown in Fig. 3B would not be obtainable.

Malik **lacks** rotating the substrate during the formation of the semiconductor layer. However, it is noted Malik discloses processes such as MBE and CVD were well known to be utilized when forming the semiconductor layer (e.g., note section 0013); furthermore, note that Malik does not specify any other deposition processes for forming the semiconductor layer; accordingly, it would have been readily obvious to utilizes at least MBE for forming Malik's semiconductor layer.

Kao **teaches** it was well known in the art that MBE (Molecular Beam Epitaxy) incorporates substrate rotation (e.g., see Col. 1, lines 21-40), wherein the rotation provides a more uniform composition of the deposited materials.

It would have been obvious to one of ordinary skill in the art to modify Christiansen by rotating the substrate because Kao teaches rotating a substrate during deposition by MBE provides a more uniform growth.

Regarding claims 28 and 29:

Malik discloses the CMP comprises a first and second step and semiconductor layer is annealed between the first and the second CMP steps, wherein the first step is considered to be "step 110" shown in Fig. 1 and the second step is considered to be "step 130" shown in Fig. 1. In other words, the current claims do not require two separate CMP processes, but rather, they only requires a CMP process comprising a first and second step, wherein no manufacturing process steps could be (or should be) excluded from being interpreted as either the first step or the second step, so long as one of the steps is a CMP process. *Specifically regarding claim 29:* Malik discloses (in Fig. 1) the "cycle" may be repeated if necessary, i.e., in a case wherein the "cycle" is repeated, the CMP comprises a first and second step and the semiconductor layer is annealed before the first CMP step, wherein the first CMP step would be "step 130" and the second step would be "step 110".

Regarding claim 30:

Malik discloses the planarization step comprises a high temperature step (i.e., an annealing step "110" in Fig. 1) that would anneal the semiconductor layer. In other words, Malik discloses the planarization comprises a CMP step, which is preceded by an annealing step; accordingly, Malik discloses a planarization comprising a high-temperature step and a CMP step, wherein the semiconductor layer is annealed during the high-temperature planarization step.

10. Claims 1, 23, 31, 32, 34 and 42-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Notsu et al. (US 2002/0146892 A1; hereinafter "**Notsu**") in view of **Nakamura** (US 2004/0060518 A1).

Regarding claims 1, 23, 31, 32, 34 and 42-44:

Notsu discloses a method for forming a semiconductor structure, the method comprising:

providing a substrate 11/12 (Fig. 1B);

forming a semiconductor layer 13/14 over a top surface of the substrate (Fig. 1B), the semiconductor layer including at least two elements (silicon and germanium), the elements being distributed to define an initial compositional variation within the semiconductor layer (paragraphs 0101-0102);

forming a protective layer 15/21 (silicon dioxide, note Fig. 1B and paragraph 0102) over the semiconductor layer 13/14 prior to annealing the semiconductor layer, wherein the protective layer is substantially inert with respect to the semiconductor layer (note the first two sentences in paragraph 0103);

bonding a top surface of the semiconductor layer 13/14 to a wafer 31 (Fig. 1C, note that although the top surface of the semiconductor layer 13/14 may not be in direct physical contact with the wafer, the top surface is nevertheless bonded to the wafer);

removing at least a portion of the substrate 11/12, wherein at least a portion of the semiconductor layer 13/14 remains bonded to the wafer after the portion of the substrate is removed;

planarizing the top surface of the semiconductor layer (note Figs. 1D-1E and in paragraph 0106, Notsu discloses polishing the remaining portions 12' such that a the top surface of the semiconductor layer is exposed, wherein the polishing would also remove a portion of the semiconductor layer, thereby providing a planarized top surface);

annealing the semiconductor layer to reduce the initial compositional variation, i.e., a layer 14" is formed from layer 13/14 by the annealing process such that the germanium concentration with the layer 14" becomes almost uniform (note paragraph 0113); and

forming a second layer 41 (Fig. 2B) over the semiconductor layer 14" subsequent to planarizing the top surface of the semiconductor layer, wherein the second layer 41 comprises a material having a lattice constant substantially different from a lattice constant of the semiconductor layer (paragraph 0114).

Notsu **lacks** rotating the substrate during the formation of the semiconductor layer. Nakamura **teaches** (in section 0005) it was well known in the art to rotate a substrate during deposition in order to obtain a more uniform growth. It would have been obvious to one of ordinary skill in the art to modify Notsu by rotating the substrate because Nakamura teaches rotating a substrate during deposition provides a more uniform growth.

11. Claims 23, 32, 33 and 36-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yamane** (in view of **Kao**) as applied to claim 1 above, and further in view of **Ohori** (5,844,260).

Regarding claims 23, 32, 33 and 36:

Yamane (in view of Kao) further discloses forming a second layer 6/11/7 (Yamane, Fig. 9) having a lattice constant substantially equal to a lattice constant of the semiconductor layer 5 (Figs. 5A, 9), wherein the second layer 6/11/7 comprises (i) a lower portion having a superlattice 6 and (ii) an upper portion 11/7 disposed over the lower portion 6, the upper portion being substantially free of a superlattice in at least the open region where gate electrode 9 is formed.

Yamane (in view of Kao) **lacks** planarizing a top surface of the semiconductor layer or planarizing the top surface prior to forming the second layer.

Ohori **teaches** that a structure similar to that disclosed by Yamane would comprise an undulated surface (Col. 8, lines 24-32) and the effects of the undulated surfaces can be diminished or eliminated by planarizing/polishing the undulated surface prior to forming a subsequent layer (Figs. 7A-7C; Col. 3, lines 39-42; and Col. 11, lines 7-24).

It would have been obvious to one of ordinary skill in the art to modify Yamane (in view of Kao) by planarizing the semiconductor layer prior to forming the second layer because Ohori teaches that planarizing the undulated surface of the superlattice layer(s) provides a flat surface for subsequent layer, thereby diminishing problems caused by the undulated surface.

Regarding claims 37-40:

Yamane (in view of Kao) **lacks** the semiconductor layer having an undulating surface. Ohori **teaches** that a superlattice structure, similar to that disclosed by Yamane, would typically have an undulating surface (Col. 8, lines 24-32) that is formed during deposition, and the undulating surface essentially results from an undulating substrate surface upon which the superlattice structure is formed (e.g., note the paragraph bridging Cols. 5-6); and the undulating surface could have an amplitude exceeding 30 microns (Col. 8, line 31). Given Ohori, one of ordinary skill in the art could have easily modified Yamane (in view of Nakamura) by specifying that the semiconductor layer has an undulating surface because Ohori shows/teaches that a superlattice structure, similar to that in Yamane, would likely have such a surface. Furthermore, since Yamane discloses a superlattice having a periodicity of about 2.5 nm (note Col. 9, lines 23-25) and Ohori teaches that the amplitude of the undulating surface could be 30 microns (or

more), the periodicity of the superlattice would obviously be less than the amplitude of the undulating surface.

Allowable Subject Matter

12. Claims 35, 45-52, 80 and 81 are allowable over the references of record.

13. Claim 35, 45-52, 80 and 81 is allowable for reasons stated in a prior Office action.

Remarks

14. Applicant's remarks/arguments have been carefully reviewed and considered, however, they are generally directed to features introduced by the amendments to claims 1-34, 36-44 and 76-79. Applicant's remarks/arguments are considered moot because the new matter introduced by the amendments to independent claims 1, 2, 16, 26 and 31 must be removed from the claims.

Conclusion

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lex Malsawma whose telephone number is 571-272-1903. The examiner can normally be reached on Mon. - Thur. (4-12 hours between 5:30AM and 10 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

March 18, 2007

LEX MALSAWMA
PRIMARY PATENT EXAMINER